ANALOG DEVICES

Blackfin® Embedded Processor

Preliminary Technical Data

ADSP-BF537 Data Sheet Addendum

FEATURES

533 and 600 MHz high performance Blackfin processors
- **Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit shifter**
- **RISC-like register and instruction model for ease of programming and compiler-friendly support**
- **Advanced debug, trace, and performance monitoring**

1.25 V to 1.3 V core V_{DD} with on-chip voltage regulation
2.5 V and 3.3 V-compliant I/O with specific 5 V-tolerant pins
182-ball and 208-ball RoHS compliant MBGA packages

MEMORY

132K bytes of on-chip memory comprised of:
- **Instruction SRAM/cache; instruction SRAM; data SRAM/cache; additional dedicated data SRAM; scratchpad SRAM**

External memory controller with glueless support for SDRAM and asynchronous 8-bit and 16-bit memories
Flexible booting options from external flash, SPI® and TWI memory or from SPI, TWI, and UART host devices
Memory management unit providing memory protection

PERIPHERALS

IEEE 802.3-compliant 10/100 Ethernet MAC
Controller area network (CAN) 2.0B interface
Parallel peripheral interface (PPI), supporting ITU-R 656 video data formats
Two dual-channel, full-duplex synchronous serial ports (SPORTs), supporting eight stereo I^2S channels
12 peripheral DMAs, 2 mastered by the Ethernet MAC
Two memory-to-memory DMAs with external request lines
Event handler with 32 interrupt inputs
Serial peripheral interface (SPI)-compatible
Two UARTs with IrDA® support
Two-wire interface (TWI) controller
Eight 32-bit timer/counters with PWM support
Real-time clock (RTC) and watchdog timer
32-bit core timer
48 general-purpose I/Os (GPIOs), 8 with high current drivers
On-chip PLL capable of 0.5× to 64× frequency multiplication
Debug/JTAG interface

GENERAL DESCRIPTION

This data sheet addendum introduces several new ADSP-BF537 models. Supported by revision 0.3 silicon, these new models will not be offered with previous revisions of ADSP-BF537 silicon. These new models are also offered as x-grade. Please see Ordering Guide on Page 6.

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter			Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	@ 533 MHz	1.20	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage[1]	@ 600 MHz	1.30	1.30	1.43	V
V_{DDEXT}	External Supply Voltage		2.25	3.3	3.6	V
V_{DDRTC}	Real Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage[2, 3]	@ V_{DDEXT} = Maximum	2.0		3.6	V
$V_{IHCLKIN}$	High Level Input Voltage[4]	@ V_{DDEXT} = Maximum	2.2		3.6	V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[5]	@ V_{DDEXT} = Maximum	2.0		5.5	V
V_{IL}	Low Level Input Voltage[2, 6]	@ V_{DDEXT} = Minimum	–0.3		+0.6	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[5]	@ V_{DDEXT} = Minimum	–0.3		+0.8	V
T_J	Junction Temperature	208-Ball Chip Scale Ball Grid Array (CSP-BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	208-Ball Chip Scale Ball Grid Array (CSP-BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	–40		+105	°C
T_J	Junction Temperature,	182-Ball Chip Scale Ball Grid Array (CSP-BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature,	182-Ball Chip Scale Ball Grid Array (CSP-BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	–40		+105	°C

[1] The regulator generates V_{DDINT} levels from 0.85 V to 1.2 V with -5% to +10% tolerance and a level of 1.25 V with -4% to +10% tolerance. For 600 MHz models only, the regulator generates a level of 1.3 V with 0% to +10% tolerance.

[2] Bidirectional pins (DATA15–0, PF15–0, PG15–0, PH15–0, TFS0, TSCLK0, RSCLK0, RFS0, MDIO) and input pins ($\overline{BR}$, ARDY, DR0PRI, DR0SEC, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF534/ADSP-BF536/ADSP-BF537 are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[3] Parameter value applies to all input and bidirectional pins except CLKIN, SDA, and SCL.

[4] Parameter value applies to CLKIN pin only.

[5] Pins SDA, SCL, and PJ4 are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[6] Parameter value applies to all input and bidirectional pins except SDA and SCL.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH} (All Outputs and I/Os Except Port F, Port G, Port H)	High Level Output Voltage[1]	@ V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5		V
		@ V_{DDEXT} = 2.5 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5		V
V_{OH} (Port F7–0)		@ V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –8 mA	V_{DDEXT} – 0.5		V
		@ V_{DDEXT} = 2.5 V ± 10%, I_{OH} = –6 mA	V_{DDEXT} – 0.5		V
V_{OH} (Port F15–8, Port G, Port H)		I_{OH} = –2 mA	V_{DDEXT} – 0.5		V
I_{OH} (Max Combined for Port F7–0)		V_{OH} = V_{DDEXT} – 0.5 V Min		–64	mA
I_{OH} (Max Total for All Port F, Port G, and Port H Pins)		V_{OH} = V_{DDEXT} – 0.5 V Min		–144	mA
V_{OL} (All Outputs and I/Os Except Port F, Port G, Port H)	Low Level Output Voltage[1]	@ V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 2.0 mA		0.4	V
		@ V_{DDEXT} = 2.5 V ± 10%, I_{OL} = 2.0 mA			
V_{OL} (Port F7–0)		@ V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 8 mA		0.5	V
		@ V_{DDEXT} = 2.5 V ± 10%, I_{OL} = 6 mA		0.5	V
V_{OL} (Port F15–8, Port G, Port H)		I_{OL} = 2 mA		0.5	V
I_{OL} (Max Combined for Port F7–0)		V_{OL} = 0.5 V Max		64	mA
I_{OL} (Max Total for All Port F, Port G, and Port H Pins)		V_{OL} = 0.5 V Max		144	mA
I_{IH}	High Level Input Current[2]	@ V_{DDEXT} =3.6 V, V_{IN} = 3.6 V		10	µA
I_{IH5V}	High Level Input Current[3]	@ V_{DDEXT} =3.0 V, V_{IN} = 5.5 V		10	µA
I_{IL}	Low Level Input Current[2]	@ V_{DDEXT} =3.6 V, V_{IN} = 0 V		10	µA
I_{IHP}	High Level Input Current JTAG[4]	@ V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V		50.0	µA
I_{OZH}	Three-State Leakage Current[5]	@ V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V		10	µA
I_{OZH5V}	Three-State Leakage Current[6]	@ V_{DDEXT} =3.0 V, V_{IN} = 5.5 V		10	µA
I_{OZL}	Three-State Leakage Current[5]	@ V_{DDEXT} = 3.6 V, V_{IN} = 0 V		10	µA
C_{IN}	Input Capacitance[7, 8]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		8	pF

[1] Applies to output and bidirectional pins.
[2] Applies to input pins.
[3] Applies to input pin PJ4.
[4] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[5] Applies to three-statable pins.
[6] Applies to bidirectional pins PJ2 and PJ3.
[7] Applies to all signal pins.
[8] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage	–0.5 V to +3.6 V
Input Voltage[1]	–0.5 V to +5.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT}+0.5 V
Load Capacitance[2]	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Underbias	+125°C

[1] Applies to 5 V tolerant pins SCL, SDA, and PJ4.
[2] For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19–1, DATA15–0, ABE1–0/SDQM1–0, CLKOUT, SCKE, SA10, SRAS, SCAS, SWE, and SMS.

PACKAGE INFORMATION

The information presented in Figure 1 and Table 1 provide details about the package branding for the Blackfin processors. For a complete listing of product availability, see Ordering Guide on Page 6.

Figure 1. Product Information on Package

Table 1. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant
ccc	See Ordering Guide
vvvvvv	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

TIMING SPECIFICATIONS

Table 2 and Table 3 describe the timing requirements for the ADSP-BF537 processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock.

Table 2. Core Clock Requirements—600 MHz Speed Grades[1]

Parameter		Internal Regulator Setting	$T_{JUNCTION} \leq 105°C$[2] Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.3 V Minimum)	1.3 V	600	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.20 V Minimum)	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.80 V Minimum)	0.85 V	250	MHz

[1] The speed grade of a given part is printed on the chip's package as shown in Figure 1 on Page 4 and can also be seen on the specific products ordering guide. It designates the maximum allowed CCLK frequency at V_{DDINT} = 1.3 V and the maximum allowed VCO frequency at any supply voltage.
[2] See Operating Conditions on Page 2.

Table 3. Core Clock Requirements—533 MHz Speed Grades[1]

Parameter		Internal Regulator Setting	$T_{JUNCTION} \leq 105°C$[2] Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.2 V Minimum)	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.80 V Minimum)	0.85 V	250	MHz

[1] The speed grade of a given part is printed on the chip's package as shown in Figure 1 on Page 4 and can also be seen on the specific products ordering guide. It designates the maximum allowed CCLK frequency at V_{DDINT} = 1.25 V and the maximum allowed VCO frequency at any supply voltage.
[2] See Operating Conditions on Page 2.

ORDERING GUIDE

Model	Temperature Range[1]	Speed Grade (Max)	Operating Voltage (Nominal)	Package Description	Package Option
ADSP-BF537BBCZ-5AV[2]	–40°C to +85°C	533 MHz	1.25 V internal, 3.3 V I/O	182-Ball CSP-BGA	BC-182
ADSP-BF537BBCZ-5BV[2]	–40°C to +85°C	533 MHz	1.25 V internal, 3.3 V I/O	208-Ball Sparse CSP-BGA	BC-208-3
ADSP-BF537KBCZ-6AV[2]	0°C to +70°C	600 MHz	1.3 V internal, 3.3 V I/O	182-Ball CSP-BGA	BC-182
ADSP-BF537KBCZ-6BV[2]	0°C to +70°C	600 MHz	1.3 V internal, 3.3 V I/O	208-Ball Sparse CSP-BGA	BC-208-3

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS compliant part.